



PATENT  
ATTY. DOCKET NO.: P67350US0

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Nam-Kyeong KIM, et al.

Group Art Unit: 2823

Serial No.: 10/025,913

Examiner: K. Nguyen

Filed: December 26, 2001

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

***REQUEST FOR RECONSIDERATION UNDER RULE 1.116***

Commissioner of Patents  
MAIL STOP AF  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the Final Office Action (Paper No. 112603) mailed December 3, 2003, Applicants request reconsideration.

The Examiner rejected claims 1-4 and 6-13 under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (AAPA) in view of U.S. Patent No. 6,320,213 to Kirlin et al. ("Kirlin"), European Patent Application EP 1 035 590 to Noh, and U.S. Publication No. 2001/0043453 to Narwankar et al. ("Narwankar").

As set forth in claim 1, the present invention is directed to a method for manufacturing a semiconductor device, comprising the steps of providing a semiconductor substrate, forming an interlayer insulating layer on the semiconductor substrate, forming a contact hole in the interlayer insulating layer, forming a plug recessed inside the contact hole, forming an

ohmic contact layer on the plug, depositing a layer selected from the group consisting of an La layer and a LaN layer on the ohmic contact layer, performing a nitridation process by a plasma treatment process to form a LaN diffusion barrier layer on the ohmic contact layer, and sequentially forming a bottom electrode, a BLT  $((\text{Bi}_x\text{La}_y)\text{Ti}_3\text{O}_{12})$  dielectric layer and a top electrode on the entire structure, wherein, in the BLT dielectric layer, the atomic concentration of Bi is 3.25 to 3.35 and the atomic concentration of La is 0.80 to 0.90. This is not shown or suggested by the prior art.

The present invention provides the La or the LaN diffusion barrier formed between the ohmic contact layer and the bottom electrode in the BLT capacitor structure. Since La, which is contained in the BLT layer, is used as the diffusion barrier in the BLT capacitor, when the La is diffused to the BLT layer during a post thermal process, a ferroelectric characteristic of the BLT layer is not degraded.

While the Examiner has rejected claim 1 on the basis of AAPA in view of Kirlin, Noh and Narwankar, Applicants maintain that there is nothing in Kirlin that would suggest to a person of ordinary skill in the art to modify what is shown in AAPA or to combine it with other references in the manner presented by the Examiner. Namely, Kirlin does not suggest that the La diffusion barrier, which is formed between the ohmic contact layer and the bottom electrode in the contact hole, *is applied in the BLT capacitor structure*. Indeed, Kirlin is completely silent as to providing any suggestion or motivation to modify or combine such reference with another reference to arrive at the La or LaN diffusion barrier in the BLT capacitor structure containing La in a dielectric layer as claimed in the present invention. Even though the La is contained in PLZT  $\{(\text{Pb},$

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La)(Zr, Ti)O<sub>3</sub>} mentioned in the art cited against the present invention, since PLZT has much worse fatigue characteristics than that of the BLT, the improvement to be obtained by using La diffusion barrier layer cannot be expected, representing an unexpected result that is patentable over the prior art.

For at least the foregoing reasons, Applicants maintain that claim 1 is patentable over the prior art and request the Examiner's reconsideration of the rejection thereof. Claims 2-4 and 6-13 are also in condition for allowance as claims that are properly dependent on an allowable base claim and for the subject matter contained therein. Favorable reconsideration and allowance of the pending claims is requested.

Should the Examiner have any questions or comments, the Examiner is cordially invited to telephone the undersigned attorney so that the present application can receive an early Notice of Allowance.

Respectfully submitted,

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TRANSMITTAL

Commissioner of Patents  
MAIL STOP AF  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a Request for Reconsideration Under Rule 1.116 for filing in the above-captioned patent application.

The fee has been calculated as shown below:

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Small Entity Rate Addit. Fee	(or)	Other Than A Small Entity Rate Addit. Fee
Total	16 -	20 =	0	x 09 = \$		x 18 = \$
Indep.	02 -	03 =	0	x 42 = \$		x 84 = \$
___ First Presentation of Multiple Dependent Claims				+130 = \$		+ 260 = \$
Total Additional Fee				\$		\$

\_\_\_ A check in the amount of \$ \_\_\_ is attached for:

XXXX If a Petition for Extension of Time is necessary and the Petition and/or the check is not enclosed, this will act as the Petition and applicant herewith petitions the Commissioner to extend the time for response and charge any fees necessary under 37 CFR 1.17 (a)(1)-(5) to Deposit Account No. 06-1358. The Commissioner is also authorized to charge payment of any other additional fees associated with this communication or credit any overpayment to Deposit Account No. 06-1358. A duplicate copy of this sheet is attached.

Respectfully submitted,  
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